REMARKS

In the present application, claims 1-51 are pending. Claims 25-38 were withdrawn from consideration. Claims 1, 2, 5-14, 17-24, 39, 40, and 43-51 are rejected. Claims 3, 4, 15, 16, 41 and 42 were objected to. Claims 1, 2, 13, 14, 39 and 40 are amended herein. As a result of this response, claims 1-24 and 39-51 are believed to be in condition for allowance.

Claim Rejections – 35 USC § 112

The Examiner rejected claims 2, 14, and 40 as being indefinite. Specifically, the Examiner asserted that the claim language "said transmitter circuitry in another IC over a second pair of adjacently disposed conductors" renders the claims indefinite. Claim 2 is amended herein to read "said transmitter circuitry in said other IC over a second pair of adjacently disposed conductors." (emphasis added). Claims 14 and 40 are similarly amended. As a result, claims 2, 14, and 40 are in condition for allowance.

Claim Rejections – 35 USC § 102

The Examiner rejected claims 1-2, 5-6, 8-9, 12-14, 17, 20, 23-24, 39-40, 43-44 and 46-47 as being anticipated by Hairapetian (6,753,700). The Examiner asserted that Hairapetian discloses "the IC are constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, voltage mode links (fig. 1, col. 1/ln. 47-col. 2/ln. 19, col. 2/ln. 40-col. 4/ln. 10)." Applicants respectively disagree with the Examiners characterization of the teachings of Hairapetian.

Claim 1 recites, in part:

> said I/O circuit being constructed with CMOS-based transistors that are **selectively interconnected together by switches to operate** as two single-ended, current or voltage mode links, **and** as a single differential current or voltage mode link.

For purposes of accuracy, it must be noted that claim 1 recites "said I/O circuit being

constructed" and not "the IC are constructed" as asserted by the Examiner. Assuming the Examiner's reference to be to the claimed "I/O circuit", Applicants respond as follows. With reference to the Examiner's citation of Fig. 1 and the accompanying description at col. 2/ln. 40-col. 4/ln. 10, it is clear that Hairapetian discloses at least one differential line 108 and a multitude of single-ended lines 110. Specifically, Hairapetian discloses "In this embodiment, bus 106 has at least one differential line 108 which is used for carrying clock signal (CKN/CKP) with several other single-ended lines 110-0 to 110-n that carry data." Hairapetian does not disclose an embodiment, either in the text or in a figure, wherein the differential and single-ended lines are "selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link" as is claimed.

Specifically, there is no disclosure or suggestion that the differential line 108 of Hairapetian ever operates as other than a differential line or that the single-ended lines 110 ever operate as other than single-ended lines. In addition, Hairapetian nowhere discloses the presence of one or more switches for selectively interconnecting the I/O circuits so as to operate the lines as either two single-ended links or as a single differential link.

In contrast, claim 1 explicitly recites that the transistors are "**selectively interconnected together by switches to operate** as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link." As this element is nowhere taught or suggested by Hairapetian, the rejection of claim 1 is respectfully traversed. As the other remaining independent claims 13 and 39 recite the above discussed element, claims 13 and 39 are likewise in condition for allowance. As claims 2, 5, 6, 8, 9, 12, 14, 17, 20, 23, 24, 40, 43, 44, 46, and 47 are dependent upon claims 1, 13, and 39, they are likewise in condition for allowance.

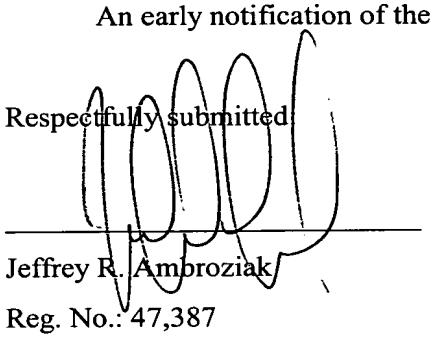
Claim Rejections – 35 USC § 103

The Examiner rejected claims 7, 10, 11, 18, 19, 21, 22, 45, 48, 49, and 51 as being unpatentable over Hairapatian in view of Pena-Finol et al. (5,832,370). The Examiner further rejected claims 12, 24, and 50 as being unpatentable over Hairapatian in view of Bjork et al. (6,009,314).

Applicants respectfully disagree with the Examiner's rejection. Neither Pena-Finol et al. nor Bjork et al. teach, disclose, or otherwise suggest "transistors that are **selectively interconnected together by switches to operate** as two single-ended, current or voltage mode links, **and** as a single differential current or voltage mode link" as claimed in independent claims 1, 13, and 39. For the reasons noted above, Hairapatian similarly fails to disclose this claimed element. As a result, the combination of Hairapatian with either Pena-Finol et al. or Bjork et al., such a combination neither suggested herein nor deemed appropriate, similarly fails to disclose the element of "transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link". While Applicants assert no further position on the accuracy of the Examiner's characterization of the teachings of Pena-Finol et al. and Bjork et al., the omission in the cited art of the above noted claimed element is sufficient, by itself, to traverse a rejection to independent claims 1, 13, and 39. As all of claims 7, 10, 11, 18, 19, 21, 22, 45, 48, 49, and 51 are dependent upon claims 1, 13, and 39, they are likewise in condition for allowance.

An early notification of the allowability of claims 1-51 is earnestly solicited.

Respectfully submitted,



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